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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,800	05/30/2001	Kazuhiko Okawa	109657	5674

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	11

DATE MAILED: 03/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/866,800	OKAWA ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *8-19 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-7 and 20-23 drawn to a MOS transistor device in Paper No. 10 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1 – 4*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Chen et al (5,166,089) in view of Honna (5,235,201) and Williams et al (5,877,534). With reference to Figure 2: Chen et al teach a semiconductor device (cf. title) comprising:

a semiconductor substrate 76/74 (cf. column 6, lines 63-64);

a MOS transistor 17 (cf. abstract, second sentence) which is formed on the semiconductor substrate and includes a first diffusion region 19 (cf. column 6, line 45);

a first isolation region 70 (cf. column 6, lines 40-43) between regions 28 and 46 (cf. Fig. 2), which isolates the MOS transistor from any other MOS transistors on the semiconductor substrate;

a second isolation region 70 (cf. column 6, lines 40-43) between regions 19 and 77 (cf. Fig. 2) and hence located between the MOS transistor and the first isolation region;

a silicide layer 68 (cf. column 6, lines 35-40) formed on a surface of the semiconductor substrate excluding at least the first and second diffusion regions (only semiconductor regions including the polysilicon gate are covered);

a second diffusion region 46 (cf. column 3, lines 55-56) which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well 74 (cf. column 6, line 64) in the semiconductor substrate.

Chen et al do not necessarily teach the third diffusion region as defined in the final limitation of claim 1. However, the creation of a Zener diode with a first diffusion region such as either source or drain of a MOS transistor and a deeper diffusion region for vertical Zener diode protection has long been known and applied in the art of protection circuits for MOSFET devices, as witnessed by Honna, who teaches a Zener diode comprising impurity diffusion region 22 and deeper diffusion region 23 (cf. column 5, lines 42-43) to form surge protection for the MOS transistor. This purpose is also the purpose of the patent to Chen et al, and the means with which this purpose is achieved can be directly implemented through standard doping techniques.

Furthermore, although Chen et al does not necessarily teach the aforementioned silicide layer to be excluded from a region connecting the first and third diffusion regions, such exclusion would be necessary for the functioning of said lateral Zener diode 27/28, as otherwise the anode and cathode of said lateral Zener diode would be short-circuited, preventing the operation of the lateral Zener diode.

Finally, although Chen et al do not specifically teach the existence of another MOSFET from which the MOSFET of claim 1 needs to be protected, it is common and standard knowledge in the art of ESD protection of MOSFET devices that electrostatic protection and hence isolation needs to be provided for MOSFET devices against the signals of other MOSFET devices, among any other source of surges. See, for instance, Williams et al, who teach (cf. Fig. 21) electrostatic discharge protection in a protection device including a PMOS and an NMOS transistor, said protection device providing protection against all combinations of voltage spikes occurring between the power supply, ground and signal inputs. It is furthermore the nature of ESD protection that the origin of the voltage spike is irrelevant for the protection. Since the protection device taught by Chen et al protects thus against any other voltage spike, it protects against those from other MOSFET devices, while devices with a plurality of MOSFET devices are common and are commonly considered in the art of ESD protection as evidenced by Williams.

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as taught by Chen et al at the time it was made so as to include a third region in accordance with the final limitation of claim 1.

With regard to claim 2: because the very purpose of the Zener diode is to give protection its breakdown voltage should be lower than that of the breakdown start voltage of the MOS transistor it is meant to protect. In other words, the further limitation is an inherent property of the Zener diode with regard to the device it is meant to protect. Therefore, the further limitation of claim 2 does not distinguish over the prior art.

With regard to claim 3: because Chen et al teaches the first and second diffusion regions 19 and 46 to be N-type (cf. column 3, lines 18 and 55) and to be located at the same main surface (cf. Figure 2) of the semiconductor substrate while the region 34 is a P well formed in the semiconductor substrate, the NPN lateral bipolar transistor of claim 3 is an inherent property of the device taught by Chen et al; Furthermore, the MOS transistor 68 having the first diffusion region is an N-type MOS transistor which sets a potential of a pad 12 to a low potential (cf. column 3, lines 6-7 and column 6, lines 35-37); and: The third diffusion region 23 (cf. column 5, line 43) as taught by Honna, which third diffusion region makes up the Zener diode by the junction with the first diffusion region, is a P-type diffusion region. This also is inherently so in order for there to be any Zener diode, because the first diffusion region 22 as taught by Honna is of N-type (cf. column 5, line 42).

In conclusion, all of the further limitations defined claim 3 are either taught in the primary reference (Chen et al) or are an inherent part of those aspects in claim 1 that had been rendered obvious in view of Honna. Therefore, the further limitations defined by claim 3 do not distinguish over the prior art.

With regard to claim 4: the further limitation defined by claim 4 stands in one-to-one relationship with the further limitation defined by claim 3 through interchange of the conductivity types of all semiconductor regions mentioned in the claim 3. The examiner takes official notice that it has long been held that simply interchanging the conductivity types of all regions involved in an invention is void of any additional patentable weight.

3. ***Claim 5*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Chen et al, Honna, and Williams as applied to claim 1 above, and further in view of Japanese patent to Uchizumi et al (JP406224376A). As detailed above, claim 1 (on which claim 5 depends) is unpatentable over Chen et al in view of Honna and Williams et al.

Neither Chen et al nor Honna nor Williams et al necessarily teach the further limitation defined by claim 5.

However, the incorporation of an additional impurity diffusion region adjacent a source or drain diffusion region and of opposite conductivity type as that of said source or drain region in a MOSFET device, such that said additional impurity diffusion region is in contact with a silicide layer has long been recognized in the art of protection devices for MOSFET's, as evidenced by Uchizumi et al, who teach an N-type conductivity diffusion region 14 in close proximity with a source region of an NMOS device by ion implantation (cf. "Constitution", lines 2-4), for the *specific purpose* of preventing latch-up protection (cf. "Purpose", lines 1-2). Said purpose is relevant to any CMOS semiconductor device and said constitution can be directly implemented in Chen et al through (e.g., phosphorus) ion implantation.

Therefore, it would have been obvious to one of ordinary skills to modify the invention of claim 1 at the time it was made so as to include the further limitation as defined by claim 5.

4. ***Claims 6 – 7*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Chen et al (5,166,089), Honna (5,235,201), and Williams et al (5,877,534) as applied to claims 3 and 4 above, and further in view of Amerasekera (5,949,094). As detailed above, claims 3 and 4 are unpatentable over Chen et al in view of Honna and Williams et al, who, however, do not necessarily teach the further limitation defined by claims 6 or 7, respectively.

However, the implementation of bipolar transistors for the *specific purpose* of protection against electrostatic discharge (ESD) has long been patented, as evidenced by Amerasekera et al, who teach a NPN bipolar transistor (N.B.: interchange of N and P regions is standardly recognized in the art as having no patentable weight) (cf. title and abstract) through N regions 18 and 20 adjacent to each other, P region 14 underneath them, and N region 106 underneath 14. The invention taught by Amerasekera pertains to an ESD protection device including the NPN bipolar transistor component, or in the alternative PNP transistor component, irregardless of the nature of the semiconductor device that is to be protected, but would readily apply to the case of a MOS transistor.

Therefore, the formation of fourth and fifth diffusion regions formed between the silicide layer and the third diffusion region so that said third, fourth, and fifth diffusion regions make up a PNP bipolar transistor would have been an obvious additional

precaution against ESD for anyone with ordinary skills in the art of semiconductor ESD protection devices. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by either claim 3 or claim 4 at the time said invention was made so as to include the further limitations defined by claims 6 and 7, respectively.

5. ***Claims 20 – 23*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Chen et al (5,166,089) in view of Williams et al (5,877,534) and Frederiksen (4,336,489). With reference to Figure 2: Chen et al teach a semiconductor device (cf. title) comprising:

a semiconductor substrate 76/74 (cf. column 6, lines 63-64);

a MOS transistor 17 (cf. abstract, second sentence) which is formed on the semiconductor substrate and includes a first diffusion region 19 (cf. column 6, line 45);

a first isolation region 70 (cf. column 6, lines 40-43) between regions 28 and 46 (cf. Fig. 2), which isolates the MOS transistor from any other MOS transistors on the semiconductor substrate;

a second isolation region 70 (cf. column 6, lines 40-43) between regions 19 and 77 (cf. Fig. 2) and hence located between the MOS transistor and the first isolation region;

a silicide layer 68 (cf. column 6, lines 35-40) formed on a surface of the semiconductor substrate excluding the first and second diffusion regions (only semiconductor regions including the polysilicon gate are covered);

a second diffusion region 46 (cf. column 3, lines 55-56) which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well in the semiconductor substrate.

Chen et al do not necessarily teach the third diffusion region as defined in claim 20. *However*, the creation of a lateral Zener diode for protection through laterally abutting an N+ doped diffusion region used to create a source or drain region with a P+ doped region has long been standard in the art of voltage breakdown protection for semiconductor circuitry, especially (C)MOS devices, as shown for instance by the patent to *Frederiksen*, who teaches in the CMOS substrate Zener cathode region 27 abutting Zener anode region 28 as part of the protection circuitry for a CMOS device for the purpose of providing a lateral Zener diode 27/28 for voltage protection. This purpose is also the purpose of the patent to Chen et al, and the means with which this purpose is achieved can be directly implemented through standard doping techniques.

Furthermore, although Chen et al does not necessarily teach the aforementioned silicide layer to be excluded from a region connecting the first and third diffusion regions, *such exclusion would be necessary* for the functioning of said lateral Zener diode 27/28, as otherwise the anode and cathode of said lateral Zener diode would be short-circuited, preventing the operation of the lateral Zener diode.

Finally, although Chen et al do not specifically teach the existence of another MOSFET from which the MOSFET of claim 20 needs to be protected, it is common and standard knowledge in the art of ESD protection of MOSFET devices that electrostatic protection and hence isolation needs to be provided for MOSFET devices against the

signals of other MOSFET devices, among any other source of surges. See, for instance, *Williams et al*, who teach (cf. Fig. 21) electrostatic discharge protection in a protection device including a PMOS and an NMOS transistor, said protection device providing protection against all combinations of voltage spikes occurring between the power supply, ground and signal inputs. It is furthermore the nature of ESD protection that the origin of the voltage spike is irrelevant for the protection. Since the protection device taught by Chen et al protects thus against any other voltage spike, it protects against those from other MOSFET devices, while devices with a plurality of MOSFET devices are common and are commonly considered in the art of ESD protection as evidenced by Williams.

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as taught by Chen et al at the time it was made so as to include all limitations of claim 20.

With regard to claim 21: because the very purpose of the Zener diode is to give protection its breakdown voltage should be lower than that of the breakdown start voltage of the MOS transistor it is meant to protect. In other words, the further limitation is an inherent property of the Zener diode with regard to the device it is meant to protect. Therefore, the further limitation of claim 21 does not distinguish over the prior art.

With regard to claim 22: because Chen et al teaches the first and second diffusion regions 19 and 46 to be N-type (cf. column 3, lines 18 and 55) and to be located at the same main surface (cf. Figure 2) of the semiconductor substrate while the

region 34 is a P well formed in the semiconductor substrate, the NPN lateral bipolar transistor of claim 3 is an inherent property of the device taught by Chen et al; Furthermore, the MOS transistor 68 having the first diffusion region is an N-type MOS transistor which sets a potential of a pad 12 to a low potential (cf. column 3, lines 6-7 and column 6, lines 35-37); and: The third diffusion region 28 (cf. column 2, line 65-68) as taught by Frederiksen, which third diffusion region makes up the Zener diode by the junction with the first diffusion region, is a P-type diffusion region. This also is inherently so in order for there to be any Zener diode, because the first diffusion region 27 as taught by Frederiksen is of N-type (cf. column 2, line 65-68).

In conclusion, all of the further limitations defined claim 3 are either taught in the primary reference (Chen et al) or are an inherent part of those aspects in claim 1 that had been rendered obvious in view of Honna. Therefore, the further limitations defined by claim 3 do not distinguish over the prior art.

With regard to claim 23: the further limitation defined by claim 23 stands in one-to-one relationship with the further limitation defined by claim 22 through interchange of the conductivity types of all semiconductor regions mentioned in the claim 22. The examiner takes official notice that it has long been held that simply interchanging the conductivity types of all regions involved in an invention is void of any additional patentable weight.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
March 7, 2002